

OpenRISC development board



An expandable OpenRISC development board for rapid prototyping of cost efficient System-on-Chip based embedded products.

FUNCTIONAL DESCRIPTION

The development board has the following functions:

FPGA

The board contains an ACTEL ProASIC3 FPGA in a PQ208 package. For configuration of the FPGA use JTAG connector JP2.

Memory

The board has 32 Mbyte of SDRAM and a 1 Mbit SPI FLASH device. There is also a SD connector, JP5, for high density FLASH cards.

IO

There are two 2x20 pin headers for external connections. The first used for ethernet signals and the second for other peripherals. A 10 pin header is used for two SPI channels and an interrupt signal.

SoC debug

The OpenRISC processor has hardware support for JTAG debugging. There is also a LVTTTL serial port used as console. Both are connected to the debug connector. On board there are also 8 LEDs that can be used for debugging purposes.

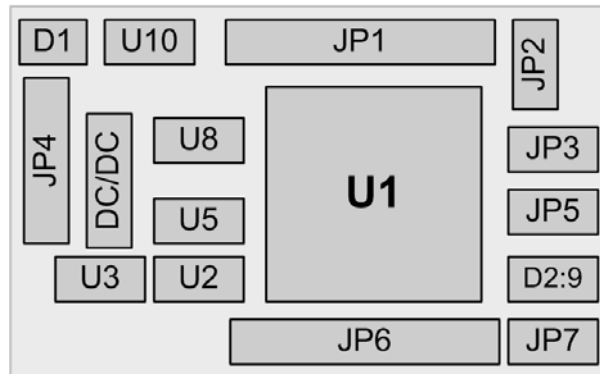
Oscillators

The board has three separate oscillators; one for SDRAM and SoC @ 66 MHz, one for ethernet SMII channels @ 125 MHz and one for audio @ 24.576 MHz. The 125 MHz clock has a clock driver supporting up to 4 SMII channels

DC/DC converter

The board requires a single 3.3 volt supply. Local converters produce the FPGA core supply, 1.5 V, and a linear converter sources the PLLs in the FPGA. All supply is available in JP4.

BLOCK DIAGRAM



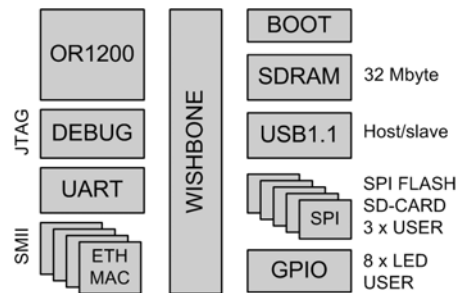
The board is 75 x 50 mm. Three connectors, JP1, JP6 and JP4, connect the CPU to a carrier board.

Bill of material:

	Component	Comment
D1	LED	On indicator
D2:9	LED	Debug
JP4	Header 1x10, 2mm	Power
JP1	Header 2x20, 2mm	Ethernet and USB
JP6	Header 2x20, 2mm	GPIO, SPI
JP2	Header 2x5	JTAG config
JP3	Header 2x5	JTAG debug
JP5	SD FLASH card connector	
JP7	Header 2x5	2xSPI + 1xGPIO
U1	FPGA ACTEL ProASIC3	PQ208
U2	Oscillator 24.576 MHz	Used for audio
U4	Oscillator 66 MHz	Used for SoC and SDRAM
U3	Oscillator 125 MHz	Used for SMII
U10	CY2509	Clock distribution
U5	SPI FLASH	1 Mbit
U8	SDRAM	32 Mbyte

SoC DESIGN

The design uses an internal wishbone SoC interconnect switching fabric. This makes the design expandable. New functions based on wishbone compatible IP can easily be incorporated



OR1200

The OR1200 is a 32 bit general purpose RISC processor. Included are 32 general purpose registers, hardware debug, instruction and data cache, instruction and data MMU, tick timer and an interrupt controller.

Boot sequence

The design has a built-in boot loader. After reset the SDRAM controller is initiated and application code is fetched from a SPI FLASH and copied to SDRAM. Upon completion the application code is executed.

Debug support

Through the JTAG interface access is granted both to CPU core and memory subsystem. Hardware debug support includes single instruction execution and breakpoints. The UART can be used as a system console. Both JTAG and UART signal is connected to the debug connector, JP3.

Ethernet

Up to four ethernet MAC units can be present in the design. Design with a single MAC can have either MII or SMII. Multiple MACs requires SMII. Each MAC has an independent MDIO channel. A carrier board with ethernet PHY, magnetics and RJ45 connectors must be used.

USB

One or more USB1.1 IP can be present. Each USB core can be used as master or slave.

SPI

Five SPI channels are present.

1. SPI FLASH
2. SD FLASH card connector (JP5)
3. connected to JP7
4. connected to JP7
5. connected to JP6

General purpose IO

A total of 32 general purpose IO signals are available. Eight of the IOs are connected to the on board LEDs. One is connected to JP7 and can be used as an interrupt source in combination with the two user SPI channels.

SUPPORT

Support is not included with the board.

Contact information: ORSoC AB

Address:
S:t Göransgatan 63
SE-112 38 Stockholm
Sweden

Website:
www.orsoc.se

Email:
info@orsoc.se

Phone:
+46 8 24 84 04